

# Fault-Management Circuit

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## Introduction

The PRM™ + VTM™ architecture provides an efficient means of providing power under rapidly varying load conditions. In the event of a fault, the VTM module shuts down automatically and remains shut down until restarted by the PRM module. The addition of a Fault-Management Circuit allows for much more flexibility in the response to a fault.

The fault-management circuit described here can be used for a PRM driving one or two VTMs in series or parallel. The circuit is compatible with the PRM / VTM families that support the ENABLE, VAUX and TM pins.<sup>[a]</sup> The circuit causes the power supply to attempt periodic restarts during the fault condition, so that power is restored automatically once the fault condition has been removed.

## Concept and Design Considerations

A fault condition could be a short circuit or overcurrent on the VTM output; an overvoltage on the input power; or a thermal fault in a VTM. If one of those conditions occurs, the VTM responds by shutting down its output. In some cases, the PRM will continue operation: for instance, if the PRM and VTM are located far apart and the VTM shuts down due to a thermal fault, the PRM would continue to regulate. To restart the power supply, it would be necessary to shut down the PRM and restart it with a pulse applied to the ENABLE pin.

In a circuit with two VTMs, there is a possibility that one VTM would shut down due to a fault and the other VTM continue to provide load current, all of which would flow through the body diodes of the faulted VTM's rectifiers. This may result in permanent damage to the faulted VTM, as well as potential overheating issues. The Fault-Management Circuit must quickly acknowledge a faulted VTM and shut down the entire system to prevent this scenario.

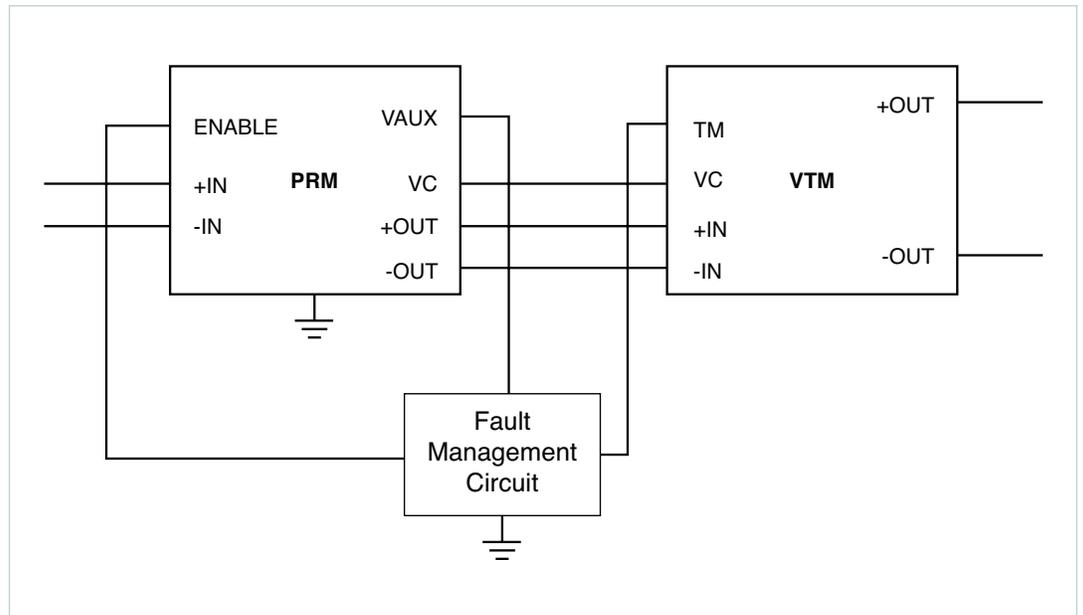
The Fault-Management Circuit senses the TM pin from the VTM; when TM goes low, indicating that the VTM has shut down, the Fault-Management Circuit shuts down the PRM by bringing the ENABLE pin of the PRM ground. Figure 1 shows a conceptual block diagram for one PRM with one VTM.

<sup>[a]</sup> A listing of devices can be found at:

<http://www.vicorpower.com/dc-dc/isolated-regulated/buck-boost-current-multipliers>

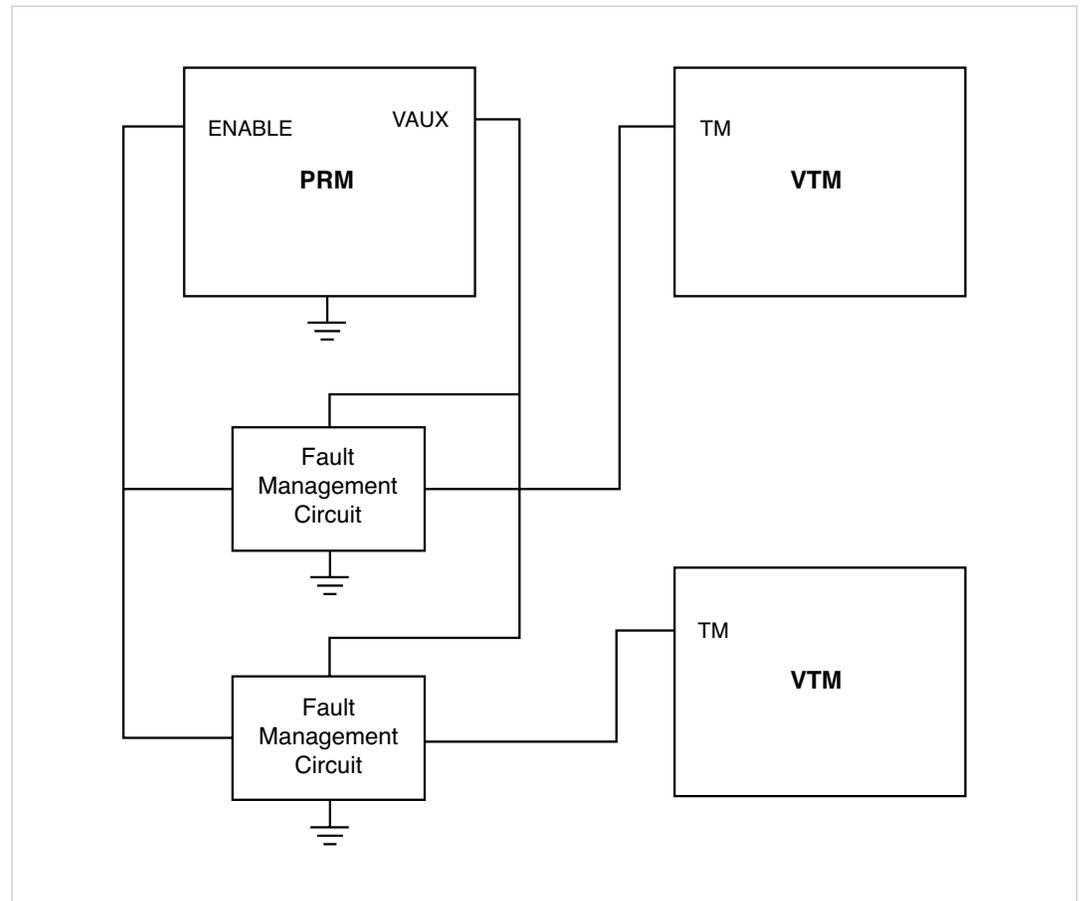
Compatible PRM's have part numbers starting with PRM; part numbers of compatible VTM's start with VTM.

**Figure 1**  
 Block Diagram of  
 Fault-Management Circuit  
 Connections with One VTM™



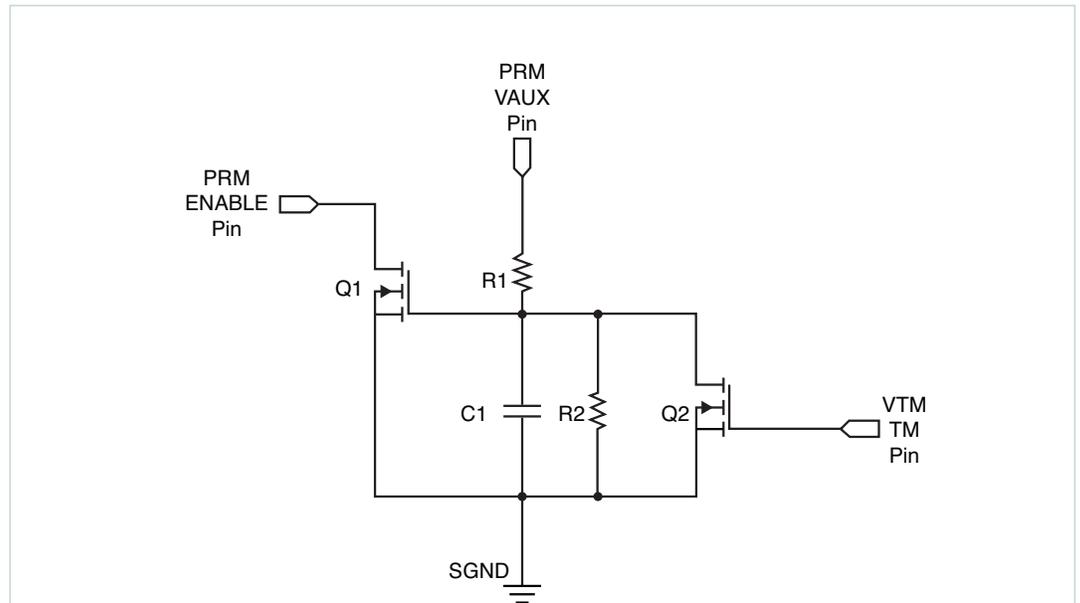
In the case of a series stack of two VTMs, two Fault-Management Circuits would be required, one for each VTM. A block diagram of this circuit is shown in Figure 2. (For the sake of simplicity, only the Fault-Management Circuit connections are shown. These connections would be the same for a series or parallel VTM configuration.)

**Figure 2**  
 Fault-Management Circuit  
 Connections for one PRM™ and  
 Two VTMs



There are many possible implementations of the Fault-Management Circuit. One implementation is shown in Figure 3. This circuit is low cost, uses little board space and satisfies the performance requirements of a broad range of systems. It gets its power and ground from the PRM's VAUX and SGND pin, respectively. The components are off-the-shelf resistors, capacitors and N-channel MOSFETs.

**Figure 3**  
Fault-Management Circuit  
Diagram



During normal operation, this circuit has no effect: TM is high, keeping Q2 turned on and Q1 turned off. On system start up, the circuit still has no effect. The PRM™ starts before the VTM™, but the RC time constant is long enough to keep the voltage on C1 too low to turn on Q2 before Q1 turns on; otherwise Q1 would turn on, bring ENABLE low and shut down the PRM again.

When the VTM detects a fault, the TM output goes low, cutting off Q2 and allowing C1 to charge through R1, causing Q1 to conduct and pull ENABLE low. With the PRM disabled, VAUX goes low, discharging C1, which cuts off Q1. ENABLE returns to a high state, allowing the PRM to start up again, which restarts the VTM. If the fault condition still exists, the VTM shuts itself down again, bringing TM low and starting the process all over. If the fault condition has been cleared, the power supply runs normally.

As long as the fault condition persists, the voltage on the ENABLE pin is a periodic series of pulses. When the circuit is cycling on and off during a fault, the duty cycle should be low enough to prevent damage to the VTM due to overheating. The period and duty cycle of the pulse train is set by the response time of the PRM-VTM loop and the RC time constant of the resistor divider R1, R2 and C1.

If there is a fault, TM goes low after about 10µs. Once the PRM has been disabled, it won't restart for 15ms, even if ENABLE is set before then. The delay from ENABLE low to TM high is typically 150µs.

The source current capability of the VAUX pin is a minimum of 5mA with 0.04µF capacitance. The source current capability of the TM pin is a maximum of 100µA with 50pF capacitance.

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## Component Selection

The Fault-Management Circuit components should be selected using the criteria below. The values in parentheses are taken from Rev 1.3 of the PRM48AH480x200A00 data sheet. Please refer to the latest version of the relevant data sheet for the appropriate values.

### Q1:

The drain to source resistance must be less than RENABLE\_EXT, (235 $\Omega$ .) This lets the transistor source enough current to bring ENABLE low.

- The absolute maximum rating of the drain to source voltage of the transistor should be greater than the maximum voltage of the PRM ENABLE pin (5.3V).
- The absolute maximum continuous drain current should be high enough to carry the maximum ENABLE current (4mA).

### Q2:

- The absolute maximum gate threshold voltage must be less than the minimum output voltage of the TM pin (2.18V).
- The absolute maximum rating of the continuous-drain current should be more than the maximum output current of the VAUX pin (5mA).
- The absolute maximum rating of Q2's drain-to-source voltage should be greater than the maximum VAUX voltage output (9.5V).

### R1 and R2:

- R1 must be sized so that the loading applied to VAUX pin does not exceed its maximum current source capability (5mA) when Q2 is ON. R1 and R2 should be sized so that loading on the VAUX pin does not exceed the maximum (5 mA) when Q2 is OFF.
- The values of R1 and R2 must be chosen so the gate voltage of Q1 stays between 5V and the maximum value of gate threshold voltage of the transistor, as listed in its data sheet.

### C1:

- The time constant formed by R1, R2 and C1 must be long enough to prevent the false start up of the PRM and VTM under normal operating conditions. The start up delay (from PRM ENABLE high to the VTM raising its TM pin) is typically 150 $\mu$ s. The RC time constant for the Fault-Management Circuit should be long enough for the gate voltage of Q1 to remain less than the minimum gate threshold voltage during start-up (See Equations 2 – 4 below).
- Too long a time constant can delay the shutting down of the PRM and VTMs after fault detection. If two VTMs are connected in series and one of them is in an overcurrent fault, the effective series output would be the output voltage of the fault-free VTM minus the forward-bias drop of the body diodes of the VTM under fault. The conduction of the fault current through the fault-free VTM's body diode must not continue long enough to cause damage to the VTM.

For most practical purposes, it's sufficient for Q1 to turn on 1 – 10ms after VAUX goes high or TM goes low. A longer delay time can be used, but to ensure reliable start up, the delay should not be less than 1ms.

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## Equations

While the PRM™ is starting from power up or restarting after a fault, during the time that ENABLE is low and  $V_{VAUX}$  is approximately 0V, the gate voltage on Q1 is:

$$V_{GQ1D} = V_{GS(TH)} (e^{-t/T}) \quad (1)$$

Where  $V_{GQ1D}$  is the gate voltage on Q1, ( $V_{GQ1}$ ) while C1 is discharging.  $V_{GS(TH)}$  is the Q1 gate-threshold voltage when Q1 is ON; it can be found in the transistor data sheet.

While Q2 is off, the gate voltage on Q1 is:

$$V_{GQ1D} = V_{TH} (1 - e^{-t/T}) \quad (2)$$

In these equations,

$$V_{TH} = V_{VAUX} \left( \frac{R2}{R1 + R2} \right) \quad (3)$$

During operation,  $V_{VAUX}$ , the output voltage of VAUX, is typically 9V when referenced to SGND.

$$T = \left( \frac{R1 \cdot R2}{R1 + R2} \right) C \quad (4)$$

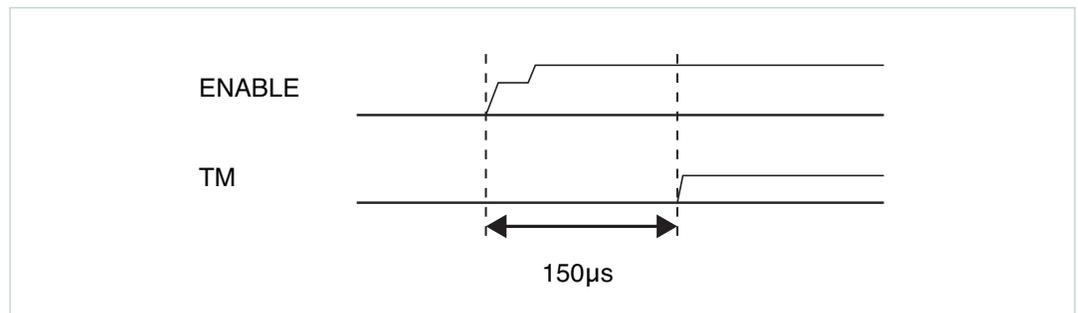
## Example

The 2N7002 is a possible selection for Q1; its minimum-gate threshold voltage is 0.8 – 1.0V. Setting  $V_{TH} = 4.5V$ ,  $V_{GQ1C} = 0.8V$  and  $t = 150\mu s$  and solving Equation 2 for the time constant T, the result is 770 $\mu s$ . For Q2, the DMN65D8L is a good choice; its maximum current and voltage meet the circuit requirements and its maximum  $V_{GS(TH)}$  is 2.0V, leaving sufficient margin for the minimum TM output of 2.18V.

Since  $V_{TH} = V_{VAUX}/2$ ,  $R1 = R2$  from Equation 3. Choosing R1 and R2 to be 49.9k $\Omega$  and using Equation 4, the minimum value of C can be found to be 33nF. For adequate safety margin, the suggested minimum value of C1 is ten times the value calculated with Equation 3, so  $C1 = 0.33\mu F$ .

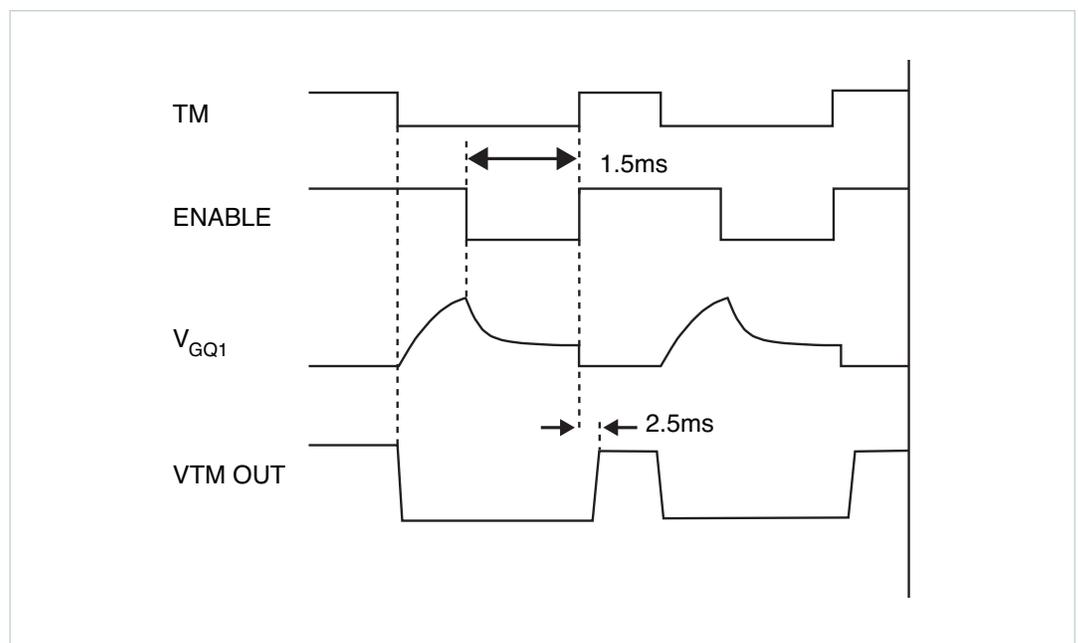
Using the values above, ENABLE and TM for a normal start up sequence are shown in Figure 4. The rising edge of ENABLE has a plateau during the time that the internal controller of the PRM is checking for faults. (See the ENABLE description in the Pin Functions section of the PRM data sheet.)

**Figure 4**  
Comparison of a  
Single Normal  
Start-Up Sequence



The fault sequence is shown in Figure 5 for one PRM™ and one VTM™. The waveforms are for a persistent fault, showing the response time, which is controlled by T (the time constant of the R1, R2, C1 circuit) and the PRM recovery time, which is 15ms. The delay from TM high to the VTM output being active is about 2.5ms. This isn't included in the start-up delay time because it doesn't affect the operation of the Fault-Management Circuit.

**Figure 5**  
Waveforms in a Fault Condition



## Conclusion

A circuit has been shown that expands the fault response capabilities of the PRM and VTM alone. The circuit described here is low cost and uses board space. It can be used where fault response parameters are not critical. The concepts shown here can be expanded on to provide for specific Fault-Management requirements.

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